**METHODS AND FINDINGS**

SELECTION ALGORITHM

**(~ referred from Methodology for the**

**evaluation and selection of microprocessors**

**for specific applications.**

**by Dr. B Srinivasan)**

Given the input characteristics of an applications and assuming that the characteristics like Hardware Characteristics (Cycle Time, Number of Primary accumulators, number of bits per accumulator, number of general register, bits per register, index register, etc.), Input and Output handling (Microprocessor with software polling, Microprocessor with vector interrupt approach, Microprocessor with direct memory access approach) Software Characteristics (Bit Manipulation, Block Transfer Instruction, Block Search Instruction, Multiplication Instruction, Stack Operations, Offset Addressing, etc.) And Interface units are available in the database for the class of microprocessors under consideration, the selection algorithm makes a search with priority on the cycle time, the processing cycle time, the I/O addressing and the method of sampling in that order and comes up with a microprocessor which is best suited for the given application. In the implementation, since the database is small, a sequential search is attempted. However, if the class of microprocessor for selection increases, database management system routines can be interfaced with the selection algorithm for data organization and retrieval. Applications in which processing time is critical in between two samples (e.g. fast Fourier transform (FFT) and control applications), in which case the cycle time and processing cycle time are important applications involving large I/O handling (e.g. air data computer, data loggers), where the number of channels and sampling frequency are important.

FFTs using the Cooley-Tukey algorithm

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The FFT algorithm computes the discrete Fourier transform of a sequence of data samples. With the Cooley Tukey algorithm the number of computations to be performed in finding the transforms is reduced. The job of the microprocessor is to compute the FFT from the following data the number of points for which the FFT is to be developed/the minimum number of points which gives the true characteristic of input is 1024; however, if the accuracy can be sacrificed, then the number of sampling points can be less) the time required to compute the transforms should be less than 620 ms each sample contains a real and an imaginary component. Based on the above input, the number of complex multiplications required by the algorithm is In/2) log2 n = 5120, when n = 1024. The number of additions required is n log2 n = 10240. Since one complex multiplication requires four real-number multiplications and two real additions, the total number of multiplications and additions required for the algorithm is 20480 + 20480. One 16 x 16-bit multiplication takes approximately four 8 x 8-bit multiplications. Therefore the number of multiplications to be done on an 8-bit microprocessor is 81920. For example, in the MC 6800 a multiplication takes 56 clock cycles 1 . When this data was fed to the selection algorithm, the algorithm chose the Intel 8086 for the FFT application. Let us validate the selection. The number of processing cycles required per transform is 81920 x 56== 4587520 {assuming the data of the MC

6800).

CRC checking in protocols

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A CRC is appended with the message to detect the corruption of information due to line noise. In this application we investigated the possibility of using a microprocessor to take care of the CRC checking. We assumed the line protocol of Digital Equipment machines, namely Digital data communication message protocol [DDCMP). DDCMP comprises various types of message. Messages are broken into packets and sent on the communication line. Every message has a header followed by 16 bits of CRC and the data part, if any. The header part of the data message is 6 bytes long and has 2 bytes of CR appended to it. When the host receives the control message, it checks for CRC and processes the information contained in the header. If the microprocessor has memory of its own to serve as a buffer for the messages, then the following operations can be carried out: Assemble the messages in the memory, Check for the CRC of the assembled messages, Send the messages with the correct CRC to the host machine. The sampling rate of the message should be at least 1200 bytes/s. Use of the algorithm given by Whiting, when coded in the assembly of the 8085, takes 1206 clock cycles and this processing must be done in less than 833 mins. With this data, the selection algorithm indicates that either an Intel 8085 or an 8086 with direct memory access sampling for data transfer can be used. Analytical calculations have also confirmed this result.